

Package Model Example

IBIS Interconnect Task Group

Randy Wolff

8/10/2016

©2016 Micron Technology, Inc. All rights reserved. Information, products, and/or specifications are subject to change without notice. All information is provided on an "AS IS" basis without warranties of any kind. Statements regarding products, including regarding their features, availability, functionality, or compatibility, are provided for informational purposes only and do not modify the warranty, if any, applicable to any product. Drawings may not be to scale. Micron, the Micron logo, and all other Micron trademarks are the property of Micron Technology, Inc. All other trademarks are the property of their respective owners.



Package Model Example

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	V _{DD}	V _{DDQ}	V _{PP}	V _{DD}	V _{SS}					V _{SS}	V _{DD}	TDO	V _{DDQ}	V _{DD}
B	V _{SS}	V _{SSQ}	DQ1	DQ0	V _{DDQ}					V _{DDQ}	DQ8	DQ9	V _{SSQ}	V _{SS}
C	V _{DDQ}	V _{DDQ}	DQ3	DQ2	V _{SSQ}					V _{SSQ}	DQ10	DQ11	V _{DDQ}	V _{DDQ}
D	V _{SS}	V _{SSQ}	EDC0	WCK01 _t	WCK01 _c					V _{DD}	V _{SS}	EDC1	V _{SSQ}	V _{SS}
E	V _{DDQ}	V _{DDQ}	DBI0 _n	V _{DDQ}	V _{SSQ}					V _{SSQ}	V _{DDQ}	DBI1 _n	V _{DDQ}	V _{DDQ}
F	V _{SS}	V _{SSQ}	DQ5	DQ4	V _{DDQ}					V _{DDQ}	DQ12	DQ13	V _{SSQ}	V _{SS}
G	V _{DD}	V _{DDQ}	DQ7	DQ6	V _{SSQ}					V _{SSQ}	DQ14	DQ15	V _{DDQ}	V _{DD}
H	V _{SS}	TMS	V _{DDQ}	RAS _n	V _{DD}					V _{DD}	CKE _n	V _{DDQ}	ZQ	V _{SS}
J	V _{DD}	V _{DDQ}	V _{SS}	A10 A0	A9 A1					BA3 A3	BA0 A2	V _{SS}	V _{DDQ}	V _{DD}
K	V _{SS}	RESET _n	V _{SS}	ABI _n	A12 A13					CK _c	CK _t	A14 A15	V _{REFC}	V _{SS}
L	V _{DD}	V _{DDQ}	V _{SS}	A8 A7	A11 A6					BA1 A5	BA2 A4	V _{SS}	V _{DDQ}	V _{DD}
M	V _{SS}	TCK	V _{DDQ}	CAS _n	V _{DD}					V _{DD}	WE _n	V _{DDQ}	TDI	V _{SS}
N	V _{DD}	V _{DDQ}	DQ31	DQ30	V _{SSQ}					V _{SSQ}	DQ22	DQ23	V _{DDQ}	V _{DD}
P	V _{SS}	V _{SSQ}	DQ29	DQ28	V _{DDQ}					V _{DDQ}	DQ20	DQ21	V _{SSQ}	V _{SS}
R	V _{DDQ}	V _{DDQ}	DBI3 _n	V _{DDQ}	V _{SSQ}					V _{SSQ}	V _{DDQ}	DBI2 _n	V _{DDQ}	V _{DDQ}
T	V _{SS}	V _{SSQ}	EDC3	WCK23 _t	WCK23 _c					V _{DD}	V _{SS}	EDC2	V _{SSQ}	V _{SS}
U	V _{DDQ}	V _{DDQ}	DQ27	DQ26	V _{SSQ}					V _{SSQ}	DQ18	DQ19	V _{DDQ}	V _{DDQ}
V	V _{SS}	V _{SSQ}	DQ25	DQ24	V _{DDQ}					V _{DDQ}	DQ16	DQ17	V _{SSQ}	V _{SS}
W	V _{DD}	V _{DDQ}	V _{PP}	V _{DD}	V _{SS}					V _{SS}	V _{DD}	MF	V _{DDQ}	V _{DD}

Data
 Addresses
 Other signal
 Supply
 Ground

■ [Interconnect Model]s

- Red: 1/4 package S-parameter
 - With VDDQ, VSS reference
 - Or no VDDQ, VSS reference
- Lt. Blue: Uncoupled S-params, VSS ref
- Blue: Lower speed Addr/Cmd
 - Fully coupled Spice subckt, VSS ref
- Purple: Low speed JTAG
 - Uncoupled RLC
- Green: PDN (no signals)
 - VDDQ, VDD, VSS reference
 - Spice coupled RLC
- Green Option 2: Full pkg coupled RLC

Discussion

- With package symmetry, S-param models are re-useable up to 4 times
 - Same S-params, but different Terminal names
 - Is there an advantage to using [Interconnect Model] names and scoping outside a set?
- What can/should be included within a single [Interconnect Model Set]?
 - Should a set contain all Pins of a package?
 - Should there be a coupled set and uncoupled set?
 - What are overlapping [Interconnect Model]s useful for?

